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Improvement in Switching Strategy used for Even Loss Distribution in ANPC Multilevel Inverter

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Abstract

This paper discusses how the even loss distribution among semiconductor devices and DC link capacitor voltage balancing by using Active Neutral Point Clamped (ANPC) multilevel inverter switching states. The main drawbacks of the Neutral Point Clamped (NPC) inverter are the unequal loss distribution among semiconductor devices and DC link capacitor voltage unbalancing. To overcome these drawbacks, switching state redundancy is required to evenly distribute the losses and the DC link capacitor voltage balances naturally under those redundant switching states. The Three Level topology is taken as the reference for NPC and ANPC multilevel inverter. This analysis is represented with the simulation results. At last the switching gate pulses from dSPACE DS 1104 and hardware implementation and the results are represented.

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*Keywords:*NPC, ANPC, dSPACE DS1104.

1. Introduction

Multilevel inverters have made revolutionary changes in the utilization of power electronics in high voltage and high power applications [1]. The basic concept involves generating output AC waveforms from small voltage steps by using series connected capacitors or isolated DC sources [1]. The small voltage steps in the output voltage produce lower harmonic distortion, lower dv/dt, lower electromagnetic interference (EMI) and higher efficiency when compared with the conventional two level voltage source inverters [1].

The 3L-NPC (Fig.2) inverter is widely used in high power medium voltage applications [2] [3]. The major disadvantage of this topology is the unequal loss distribution among the switches. However it also generates unequal

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junction temperature distribution which confines the inverter maximum output power [4]. Moreover as the levels of the inverter increase the unequal switching of the semiconductor devices also increase and so the voltage unbalance between the DC link capacitors also increases.

The three level active neutral point clamped (3L-ANPC) inverter shown in Fig.1 is an attractive topology which can overcome the unequal loss distribution problem of the 3L-NPC inverter and improve the power ability [5]. In 3L-ANPC inverter topology two auxiliary switches are added for the purpose of clamping instead of clamping diodes as in 3L-NPC. These auxiliary switches are introduced to ensure the equal voltage sharing between the main and auxiliary switches. Moreover in unlike NPC inverter, in ANPC inverter the DC link capacitor voltage will naturally balance under normal operation of inverter. This is because of increased switching redundancy due to adding the clamping switches instead of clamping diodes.

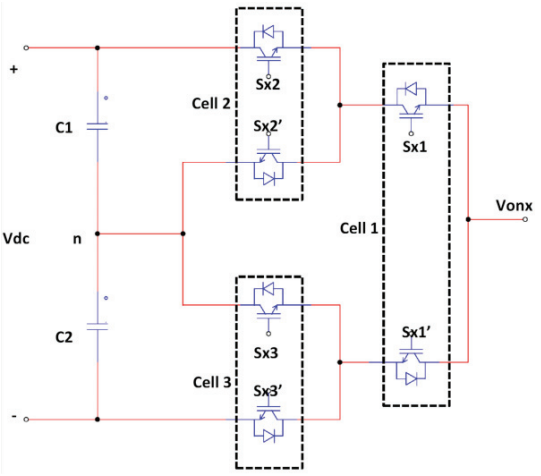

Fig. 1. 3L-Active NPC multilevel Inverter

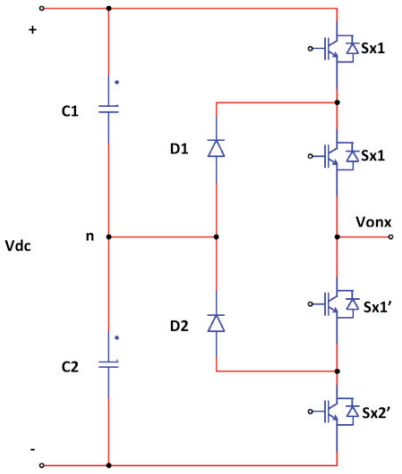

Fig. 2. 3L-NPC multilevel inverter

2. Three Level Neutral Point Clamped Multilevel Inverter (3L-NPC)

A single phase 3L-NPC is shown in Fig .2. Where x represents the phase a, b or c. The switches (Sx1, Sx1'), (Sx2, Sx2') are the complimentary switching pairs. The output is taken with reference to the neutral point n. i.e. V_{oxn}. Diodes Dx1 and Dx2 are the clamping diodes. Capacitors c1 and c2 are the DC link capacitors that will divide the input voltage V_{dc} equally. The switching sequence for producing three level output is shown in Table 1.

Table 1. Switching States of 3L-NPC

Switches				Voltage Level
Sx1	Sx2	Sx1'	Sx2'	
1	1	0	0	+Vdc/2
0	1	1	0	0
0	1	1	0	0
0	0	1	1	-Vdc/2
1=ON, 0=OFF				

For producing voltage level +Vdc/2 switches Sx1 and Sx2 are to be turned on and its complimentary switches (Sx1' & Sx2') will remain turned off at this time. So the upper DC link capacitor C1 will connect to the positive of the supply compared to the neutral point and across the load +Vdc/2 is obtained. For producing zero voltage level switches Sx2 and Sx1' are turned on. There are two current paths for the flow of current. First is Dx1 to Sx2 and to the neutral point. Second is Dx2 to Sx1' and to the neutral point. At this time the diodes Dx1 and Dx2 will carry the

neutral point current. Ideally under the balance load condition the neutral point potential will be at zero. Hence zero output voltage level is achieved. For producing voltage level –Vdc/2 switches Sx1' and Sx2' are turned on. Now the lower capacitor will supply to the load but in the reverse direction and –Vdc/2 output voltage level is achieved.

From the operation of 3L-NPC multilevel inverter we can analyse that the turn ON time or conduction time of the middle two switches i.e. Sx2 and Sx1' are comparatively higher than the upper and lower switches i.e. Sx1 and Sx2'. Here is the concept of unequal switching of semiconductor devices which can cause of unequal junction temperature as well as unbalancing DC link capacitors. In higher than the three level inverter, the middle DC link capacitors will discharge more compared to the upper DC link capacitors.

3. Three Level Neutral Point Clamped Multilevel Inverter (3L-NPC)

A single phase 3L-ANPC is shown in Fig. 1. Where x represents the phase a, b or c. It can be regarded as the combination of three two-level cells namely cell1, cell 2, and cell 3. Switches (Sx1, Sx1'), (Sx2, Sx2'), and (Sx3, Sx3') are complementary switch pairs of each cell. The output is taken with reference to the neutral point n. i.e. Voxn. The switching sequence for producing three level output voltage is shown in Table 2.

Table 2. Switching states of 3L-ANPC

Switches						Voltage
Sx1	Sx2	Sx3	Sx1'	Sx2'	Sx3'	Level
1	1	1	0	0	0	+Vdc/2
1	0	0	0	1	1	0
1	0	0	0	1	0	0
0	0	1	1	0	0	0
0	1	1	1	0	0	0
0	0	0	1	1	1	-Vdc/2
1=ON, 0=OFF						

For producing voltage level +Vdc/2 Sx1, Sx2 and Sx3 are turned ON. Here Sx3 is ON and ensures the equal voltage sharing between the off state switches i.e. Sx2' and Sx3'. For the zero voltage stage there are four redundant switching states with different current paths. The phase current flows through the upper path in both direction when Sx2', Sx1 and Sx3' are turned ON. While through the lower path when Sx1', Sx2 and Sx3 are turned ON. Neutral current only, will flow through both the paths in zero voltage state. The even distribution of switching losses in the 3L-ANPC inverter is achieved by selecting upper or lower current paths. For the voltage level –Vdc/2 switches Sx1', Sx3' and Sx2' are turned on. Here again the switch Sx2' ensures the equal voltage sharing between the Sx2 and Sx3.

From the operation of 3L-ANPC multilevel inverter we can analyse that the turn ON time or conduction time is equal for all the switches. Hence there is the equal switching of each semiconductor device and it will also help in balancing of DC link capacitors by choosing the proper switching sequence.

4. Comparative Analysis of Switching Losses in 3L-NPC and 3L-ANPC Multilevel Inverter With Simulation Results

This section discusses the control strategy of PWM and the MATLAB simulation results of three levels NPC and ANPC multilevel inverter's comparative analysis of losses across the semiconductor devices.

4.1 Control Strategy

The control strategy that is used in this paper for simulation is phase shifted carrier based pulse width modulation (PS-PWM) shown in Fig. 3. For the three level output there are two carriers required which are phase shifted by 180º. These carriers are to be compared with the 50Hz sinusoidal reference signal.

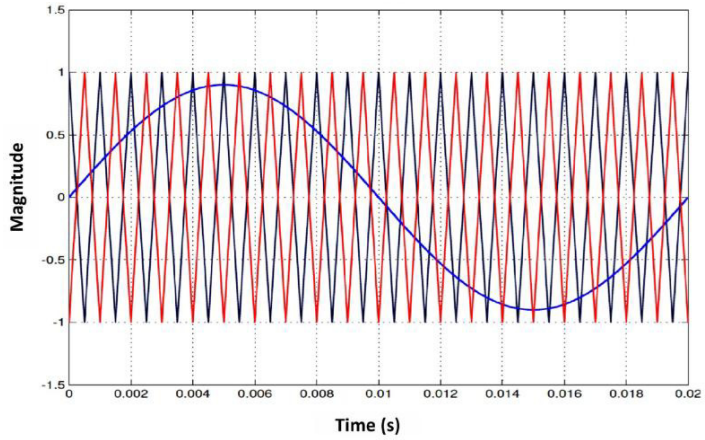

Fig.3. Phase Shifted Pulse Width Modulation (PS-PWM) technique

The resultant output pulses that are generated by carrier 1 is given to the switches Sx1 and its complementary pulses given to the Sx1'. Similarly the carrier 2 pulses is given to the switches Sx2 and Sx3 and their complementary pulses given to the Sx2' and Sx3'.

4.2 MATLAB simulation results discussion

From the simulation results of 3L-NPC with resistive load, it is clear that the voltage stresses are high across the switches Sx2 and Sx1' compared to Sx1 and Sx2' i.e. middle switches in 3L-NPC. It will produce the uneven distribution of switching losses among the semiconductor devices. So, the switch ratings for the middle switches in NPC multilevel inverter must be taken higher than the upper and the lower switches to match the equal switching losses. The uneven distribution will also cause for unbalance in DC link capacitors in higher levels of the multilevel inverter. By comparing the results of voltage across the switches in 3L-ANPC with resistive load to that of 3L-NPC, it is clear that the loss distribution among the semiconductor devices is even in Active Neutral Point Clamped Multilevel Inverter. So, the inverter maximum power can be achieved. Fig. 4 shows that the output phase voltage is well balanced .

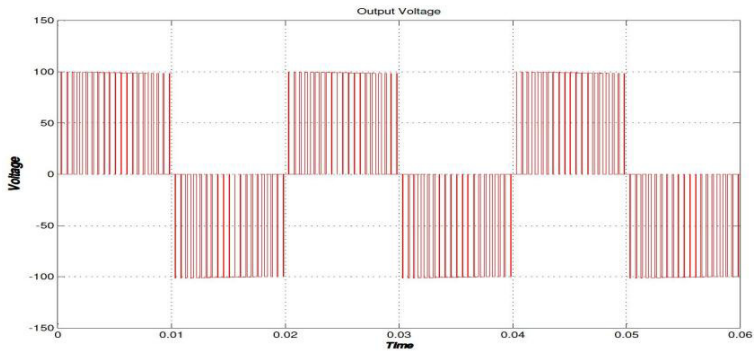

Fig.4. Output Voltage of 3L-ANPC MLI

It is also beneficial for higher levels of multilevel inverter for natural balancing of DC link capacitors because there are switching redundancies in ANPC multilevel inverter. However, this will cost extra switches instead of diodes. But the rating of switches can be reduced by even distribution of losses and the switches can be provided with the same ratings.

5. Hardware Implementation & Results

5.1 Block diagram of dSPACE DS 1104

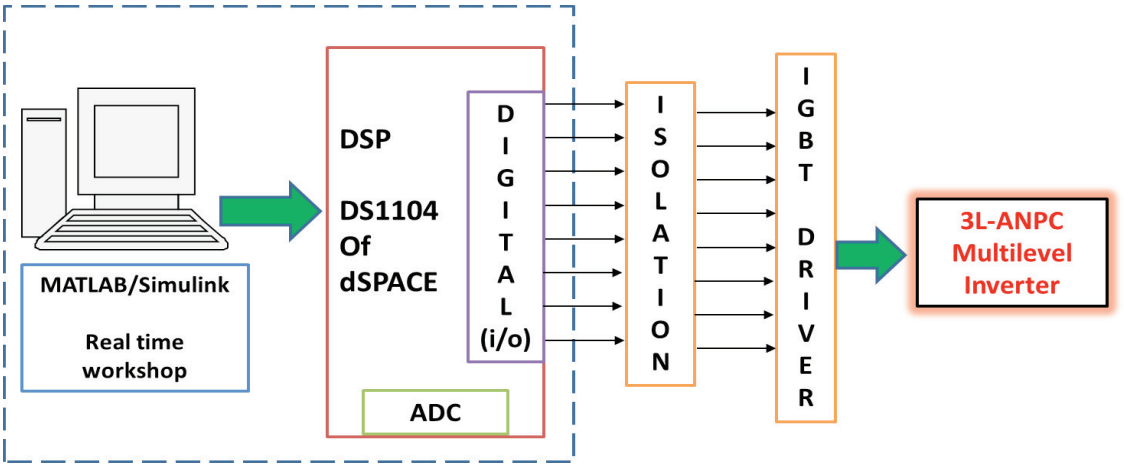

Fig .5. Block diagram of dSPACE DS 1104

For the generating gate pulses of 3L-ANPC MLI, dSPACE DS 1104 controller board is used which is shown in Fig. 5. It will control the inverter output voltage or frequency according to the MATLAB Simulink model. Feedback can be provided to dSPACE controller through the ADC I/O channel provided.

Here, open loop hardware is implemented and there is no feedback provided to ADC. From the digital i/o, the control gate pulses are got and given to the inverter through isolation and driver circuits.

5.2 Hardware results and discussions

The 3L-ANPC multilevel inverter with resistive load is done for the analysis of switching loss distribution and natural balancing of DC link capacitors.

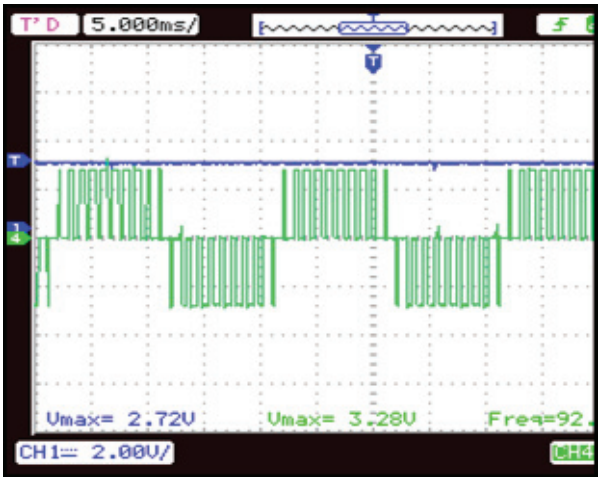

Fig. 6. DC link Voltage across capacitor C1

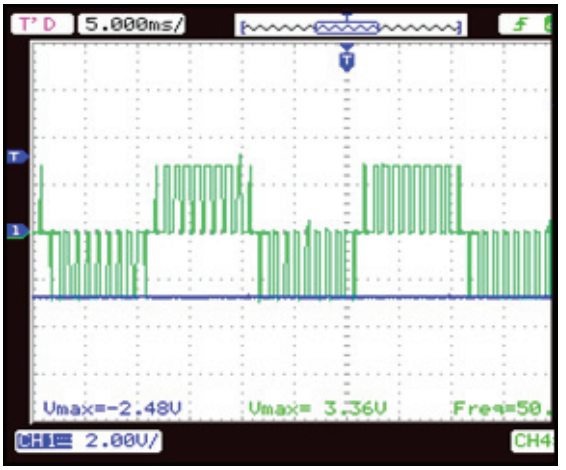

Fig. 7. Voltage across DC link capacitor C2

Fig. 6 and Fig. 7 show the voltage across the DC link capacitors C1 and C2 are well balanced under the switching redundancy. Fig. 8 shows the full hardware setup of 3L-ANPC MLI.

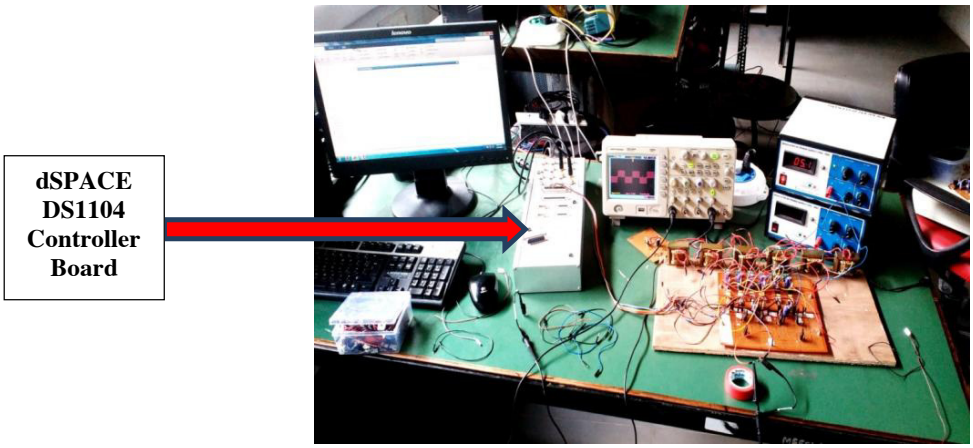

Fig. 8. Full hardware setup of 3L ANPC multilevel inverter

6. Conclusion

The paper discusses about the different types of multilevel inverter and during switching, how are the switches subjected to voltage stress. Simulation for the same is carried out in MATLAB simulink. Results show that switching state redundancy is required to evenly distribute the losses in ANPC multilevel inverter. The switching strategy is implemented in hardware using dSPACE DS 1104 and the results are verified.

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